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Enclosed are:

[**X**] Specification, Claim(s), and Abstract (39 pages).

[**X**] Formal drawings (9 sheets, Figures 1-15).

[**X**] Declaration and Power of Attorney (2 pages).

[**X**] Assignment of the invention to NEC CORPORATION.

[**X**] Assignment Recordation Cover Sheet.

[**X**] Claim for Convention Priority w/ 1 certified document.

[**X**] Information Disclosure Statement.

[**X**] Form PTO-1449 with copies of 3 listed reference(s).

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SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to a semiconductor device having an input protection circuit section or an output protection circuit section between an input/output terminal and an internal circuit to prevent the electrostatic discharge(ESD).

2. Description of the related Art

In a semiconductor integrated circuit device, an input protection circuit section or an output protection circuit section (referred to as an input/output protection circuit section, hereinafter) is set between an input terminal or an output terminal or an output terminal (referred to as an input/output terminal, hereinafter) and an internal circuit in order to protect circuit elements inside from failure which may be brought about by an ESD or the like applied to the input/output terminal.

An input/output protection circuit section itself is generally composed of CMOSs (Complementary Metal-Oxide-Semiconductor) in each of which an N-channel MOSFET (Field Effect Transistor) and a P-channel MOSFET are connected in series between the supply voltage V_{DD} and the ground voltage GND. Fig. 14 is a diagram of an input protection circuit composed of CMOSs and Fig. 15, a diagram of an output

protection circuit composed of CMOSs. Now, referring to the drawings, an example of a conventional input protection circuit section composed as shown in Fig. 14 is described below.

Fig. 6 is a plan view showing a conventional input protection circuit section composed of CMOSs and Fig. 7, a cross-sectional view showing the portion A-A' of Fig. 6. As shown in Fig. 7, on the surface of a P-type silicon substrate 20, an N-type well 1b and a P-type well 2 is formed. In the region where the P-type well 2 is formed, an N-channel MOSFET comprising a gate electrode 6, a source region 3c and a drain region 3b is formed. In the periphery of the N-channel MOSFET formation area, a P-type dopant diffusion region 4a is set (Fig. 6), and thereby the electric potential of the P-type well 2 is defined. The P-type dopant diffusion region 4a and the source region 3c, set separated by an element isolation film 10, are both connected with a ground terminal 9 (GND). The drain region 3b is connected with an input terminal 7.

Meanwhile, in the region where the N-type well 1b is formed, a P-channel MOSFET comprising a gate electrode 5, a source region 4c and a drain region 4b is formed. In the periphery of the P-channel MOSFET formation area, an N-type dopant diffusion region 3a is set (Fig. 6), and thereby the electric potential of the N-type well 1b is defined. The N-type dopant diffusion region 3a and the source region 4c,

set separated by an element isolation film 10, are both connected with a supply terminal 8 (V_{DD}). The drain region 4b is connected with an input terminal 7.

Further, for the purpose of lowering electrical resistance, silicide layers13 are formed over the surfaces of the source-drain regions and such, in every transistor.

Next, operations that take place on application of an external surge to the input terminal 7 are described. Firstly, operations that the N-channel MOSFET makes when an external surge is applied to the input terminal 7 with a negative voltage with respect to the ground terminal 9 are described. A forward voltage is, in this instance, applied to the PN-junction between the drain region 3b (N-type) and the P-type well 2 and the PN diode is turned on in the forward direction so that the negatively polarized surge flows down from the input terminal 7, through the drain region 3b and the P-type well 2, to the ground terminal 9. Next, operations produced when an external surge is applied to the input terminal 7 with a positive voltage with respect to the ground terminal 9 are described. In this case, a positive voltage with respect to the P-type well of the N-channel transistor is applied to the drain. When this voltage exceeds a certain value, an avalanche breakdown takes place in the vicinity of the drain region 3b. After the breakdown, a current flows from the drain region 3b to the P-type well 2 and this current leads the P-type well 2

to have a positive electric potential, which results in turning-on of an NPN parasitic bipolar transistor in which the drain region 3b, the P-type well 2 and the source region 3c act as a collector, a base and an emitter, respectively. The surge, then, flows from the internal terminal 7, through the drain region 3b, the P-type well 2 and the source region 3c, and consequently to the ground terminal 9. The operations described above are further described with reference to Fig. 9. In Fig. 9, when the drain voltage reaches the breakdown voltage V_B, the breakdown takes place and, after that, the voltage rises, up to the trigger voltage V_{t1}. Once the voltage reaches V_{t1}, the NPN parasitic bipolar transistor is turned on, and the voltage drops to the snap-back holding voltage V_S. When the current and the voltage rise again and reach the value of the current I_{t2} and the value of the voltage V_{t2}, respectively, the transistor is driven to a failure.

While only operations of the N-channel MOSFET are described so far, the P-channel MOSFET operates in a similar fashion. In short, when an external surge is applied to the internal terminal 7 with a positive or a negative voltage with respect to the supply terminal 8, either the PN junction in the forward direction is turned on, or alternatively, a lateral parasitic bipolar transistor is turned on. In either way, the surge flows down to the supply terminal 8 and thereby the internal circuit is

protected.

However, the protection circuit section described above has the following problem, originating from the fact that V_{t2} (the transistor failure voltage) is lower than V_{t1} (the trigger voltage), as seen in Fig. 9.

The protection circuit section is normally composed of a plurality of transistors, and each transistor has a slightly different own trigger voltage of the snap-back. As a result, when the snap-back operation starts, it is made by not all but only some of the transistors. However, the voltage of the input/output terminal, thereat, falls back to the snap-back holding voltage V_S of these transistors, and, then, recovers only up to V_{t2} of these transistors. With respect to the rest of the transistors, therefore, the snap-back operation cannot be induced, since the drain voltage does not exceed their own V_{t1}. In consequence, the surge always flows down only to the transistors making the snap-back operation and leads them to failures, which lowers the protective capability of the protection circuit section. In recent years, with the object of reducing the parasitic resistance and the like, metal silicide films are often formed over the surfaces of the source-drain regions of the transistors and such. In such a case, the surge current is drawn to the vicinity of metal silicide layers of low resistivity so that the above problem becomes more pronounced.

Although the above description is made, with N-channel transistors considered, the similar can be applied to the case of P-channel transistors.

To overcome the above problem, a high-resistance region is often set by the side of the drain region of the transistor. Fig. 10 and Fig. 11 show the protection circuit section disclosed in Japanese Application Laid-open No. 173070/1998. In this protection circuit section, an N-type well 1c is formed by the side of a drain region 3b of an N-channel MOSFET, and a control electrode 6a is set in order to define the electric potential of the N-type well 1c (Fig. 11). With the N-type well resistance 14, the resistance between the input terminal 7 and the ground terminal 9 increases and the relationship between the drain voltage V_{ds} and the drain current I_{ds} becomes the one as shown in Fig. 12. In the drawing, the dotted line represents the profile of the conventional technique and the solid line, the profile of the protection circuit section of Fig. 11. In the profile of the solid line, the value of dI_{ds}/dV_{ds} between V_S and V_{t2} is made smaller by the presence of the N-type well resistance 14, and, consequently, V_{t2} increases to establish the relationship $V_{t1} < V_{t2}$. Under this condition, even if only some of the transistors are induced to make the snap-back operation first, the rest of the transistors are also induced to make the snap-back operation in the similar fashion, as the drain voltage, after the snap-back,

increases from V_S to V_{t2}, and, thus, a plurality of transistors all function alike. Therefore, more than sufficient surge-proof (ESD (Electrostatic Discharge)-proof) can be secured, without lowering protective capability thereof. In this way, the use of a method in which a high-resistance region is set can make a plurality of transistors operate all alike and heighten the reliability of the protection circuit section. Accordingly, the above method is widely utilized for the protection circuit sections.

Yet, this method wherein a high-resistance region is formed still has problems in the following points. Firstly, an addition of a high-resistance region lowers the driving capability of the protection circuit section and worsens the quality of high-speed operation thereof. Secondly, as the drain current of the transistor becomes smaller due to the presence of the high-resistance region, the transistor size required to secure a prescribed driving current in the output circuit or the like becomes larger. Thirdly, in order to dispose a resistance element between a gate and a contact in the drain region of the protection circuit section, the spacing between the gate and the drain must be set wider, which hinders the LSI (Large Scale-Integrated circuit) miniaturization.

Meanwhile, for the arrangement of the protection circuit section in the LSI, a form in which a protection circuit section composed of complementary field effect

transistors is set between the supply voltage V_{DD} and the ground voltage GND is generally utilized. This arrangement can make a surge flow down to the GND or the V_{DD} efficiently and, therefore, can attain a good ESD-proof and maintain the quality for the protection circuit response.

When the protection circuit section composed of complementary field effect transistors is employed, prevention of latch-up becomes another important technical problem. As a prevention measure of latch-up, it is well known that setting a dopant high-concentration region beneath wells in the transistor formation area is effective (Japanese Patent Application Laid-open No. 321150/1997). Fig. 13 shows an example of the CMOS with such a structure. Nevertheless, when such a structure is employed for the protection circuit section, although the latch-up-proof certainly improves through a reduction of the shunt resistance, a problem of a decrease in the ESD-proof arises. The explanation lies in the fact that, with reducing the shunt resistance, the current amplification factor of the parasitic bipolar transistor decreases and this makes the parasitic bipolar operation difficult to induce. In effect, this structure has an adverse effect on the protection circuit section that makes use of parasitic bipolar operations. Accordingly, a technique that can improve the latch-up-proof while maintaining the ESD-proof of the protection circuit section has been very much waited for.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device that has an excellent driving capability and a good quality for high-speed operation, with ESD-proof as well as latch-up-proof amply provided, while the element size of an input/output protection circuit section thereof successfully reduced.

In light of the above problems, the present invention provides a semiconductor device having an input/output protection circuit section on a semiconductor substrate; wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type and a gate electrode that is set in the region sandwiched between these layers; and

a dopant diffusion region of second conductive type is set at a distance from the region where said plurality of field effect transistors are formed; and

while said dopant diffusion region is connected with a reference potential, the second diffusion layer is connected with an input/output terminal section; and

under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

Because the input/output protection circuit section contained in a semiconductor device of the present invention has, under the first diffusion layer, a first conductive type well with a lower dopant concentration than the first diffusion layer, the base potential of a lateral parasitic bipolar transistor that is composed of a first and second diffusion layers and a region sandwiched between these layers can be readily raised, and the snap-back, easily induced thereto. This enables the present protection circuit to take a lower value of the trigger voltage V_{t1} than the conventional ones. In consequence, the amount of the injection current necessary to make the parasitic bipolar transistor operate can be reduced, which leads to a higher speed of response. Furthermore, as the condition $V_{t1} < V_{t2}$ can be established, a plurality of transistors composing the protection circuit section all operate alike so that it can be prevented that the surge flows down only to some specific transistors. Therefore, improvements on the ESD-proof as well as on the reliability of the protection circuit section can be attained.

Further, the semiconductor device described above has the structure in which the second diffusion layer is connected with the input/output terminal section, that is, the field effect transistor is directly connected with the input/output terminal section. In conventional techniques, an input/output terminal section is often connected through

a high-resistance region to a transistor section, as shown in Fig. 11. In contrast with this, the present invention has a structure in which an input/output terminal section and a transistor section are directly connected with each other. This allows the first conductive type well to demonstrate its function fully and facilitates the parasitic bipolar operations. Moreover, as the surge is directly applied to the drain without passing through a resistance, the response of the protection circuit becomes faster. Because a resistance is not passed through, with a such a connection, the drain current of the transistor is not lowered, and a sufficient driving current can be readily secured even in the output circuit or the like. Further, since no additional resistance element is disposed between a gate and a contact in the drain region of the protection circuit section, the spacing between gates can be narrowed and the element size of the input/output protection circuit section can be reduced, which is an advantage to make miniaturization of the LSI. Regarding the second conductive type dopant diffusion region, one or more regions may be formed for the whole of a plurality of field effect transistors. Further, in respect of the geometrical arrangement, the second conductive type dopant diffusion region may be formed without any specific limitation, as long as it is formed at a distance from the region where a plurality of field effect transistors are formed. For

instance, it can be formed to encircle a plurality of field effect transistors all together like the P-type dopant diffusion region 4a of Fig. 1.

In the semiconductor device described above, it is preferable to have a structure, in which the gate electrode and the dopant diffusion region of second conductive type are placed over the second conductive type well that is formed on the surface of the semiconductor substrate; and the bottom of the first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well. In other words, it is preferable that the gate electrode of the field effect transistor and the dopant diffusion region of second conductive type are formed over the second conductive type well, and the first conductive type well has a depth not less than the depth of the second conductive type well. With such a structure, after the breakdown of the drain section, a current flows through the semiconductor substrate that has a higher resistance than the second conductive well, which facilitates the potential of the base region of the aforementioned lateral parasitic bipolar transistor to rise and, therefore, makes the trigger voltage V_{t1} lowered more effectively. This further improves the quality of the response of the protection circuit section as well as the ESD-proof.

Further, the present invention provides a semiconductor device having, on a semiconductor substrate, an input/output protection circuit section that contains a complementary field effect transistor; wherein:

said complementary field effect transistor is composed of a first field effect transistor having a first and second diffusion layers of first conductive type and a gate electrode that is set in the region sandwiched between these layers and a second field effect transistor having a third and fourth diffusion layers of second conductive type and a gate electrode that is set in the region sandwiched between these layers; and

a first dopant diffusion region of second conductive type is set at a distance from the region where said first field effect transistor is formed and a second dopant diffusion region of first conductive type is set at a distance from the region where said second field effect transistor is formed; and

the first dopant diffusion region is connected with a first reference potential; the second dopant diffusion region, with a second reference potential; and the second diffusion layer and the fourth diffusion layer are each connected with an input/output terminal section; and

under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

Because the input/output protection circuit section of this semiconductor device comprises a complementary field effect transistor, a surge can flow down through a plurality of lines efficiently so that the quality of high-speed operation of the protection circuit as well as the ESD-proof can be further improved. For the purpose of improving the reliability of the protection circuit, it is preferable that a plurality of N-channel type field effect transistors are provided to compose a complementary field effect transistor.

In this semiconductor device, it is preferable to have a structure, in which the gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate; and the bottom of the first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well. In other words, it is preferable that the gate electrode of the first field effect transistor and the first dopant diffusion region are formed over the second conductive type well, and the first conductive type well has a depth not less than the depth of the second conductive type well. With such a structure, after the breakdown of the drain section, a current flows through the semiconductor substrate that has a higher resistance than the second conductive well, which facilitates the potential of the base

region of the afore-mentioned lateral parasitic bipolar transistor to rise and, therefore, makes the trigger voltage V_{t1} lowered more effectively. This further improves the quality of the response of the protection circuit section as well as the ESD-proof.

Further, if this semiconductor device has, in addition, a structure in which, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well; and the bottom of the first conductive type well is formed at the same depth as the bottom of the dopant high-concentration region or at a level deeper than the bottom of the dopant high-concentration region, a protection circuit section having a good ESD-proof, together with a good latch-up-proof, can be obtained. As described above, it is well known that setting a dopant high-concentration region at the bottom of the wells can reduce the shunt resistance and improve the latch-up-proof. However, with reducing the shunt resistance, the current amplification factor of the parasitic bipolar transistor decreases, which makes the parasitic bipolar operations difficult to induce and gives rise to a problem of lowering the ESD-proof. The present invention, hereat, overcomes the above problem by setting a first conductive type well that reaches a depth equal to or deeper than that of the bottom

of the dopant high-concentration region. Fig. 3 shows an example with the structure described above, and an N-type well 1a reaching the same depth as the dopant high-concentration region 16 is set therein. With such an N-type well 1a being set, after the breakdown of the drain region 3b, a current starts flowing down through the semiconductor substrate 20 that has a high electric resistance. This facilitates the electric potential of the base region 2 of the lateral parasitic bipolar transistor to increase and, at the same time, can reduce the trigger voltage V_{t1} so that the ESD-proof may be improved. Meanwhile, in the internal circuit region (not shown in the drawing), because the shunt resistance is made smaller by the dopant high-concentration regions 15 and 16, the proof can be a good deal improved against latch-up that may occur between the input/output protection circuit section and the internal circuit region.

In the present invention, it is preferable that the field effect transistor to which a first conductive well is additionally set is an N-channel type field effect transistor. This results from the fact that an NPN-type parasitic bipolar transistor has a higher current amplification factor and besides, high-speed operations thereof have a better quality than those of a PNP-type one.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic top plan view showing a

protection circuit section of a semiconductor device in accordance with the present invention.

Fig. 2 is a schematic cross-sectional view showing the portion A-A' of Fig. 1.

Fig. 3 is a schematic cross-sectional view showing a protection circuit section of another semiconductor device in accordance with the present invention.

Fig. 4 is a diagram showing the I-V characteristic of a transistor in a protection circuit section of a semiconductor device in accordance with the present invention.

Fig. 5 is a view in explaining the current path of a surge current in an input protection circuit section of a semiconductor device in accordance with the present invention.

Fig. 6 is a schematic top plan view showing a protection circuit section of a conventional semiconductor device.

Fig. 7 is a schematic cross-sectional view showing the portion A-A' of Fig. 6.

Fig. 8 is a schematic cross-sectional view showing a protection circuit section of an Comparative Example.

Fig. 9 is a diagram showing the I-V characteristic of a transistor in a conventional protection circuit section.

Fig. 10 is a schematic top plan view showing a protection circuit section of another conventional

semiconductor device.

Fig. 11 is a schematic cross-sectional view showing the portion B-B' of Fig. 10.

Fig. 12 is a diagram showing the I-V characteristic of a transistor in another conventional protection circuit section.

Fig. 13 is a view in explaining a prevention measure against latch-up in a CMOS.

Fig. 14 is a diagram showing an input protection circuit.

Fig. 15 is a diagram showing an output protection circuit.

DETAILED DESCRIPTION OF THE PREFFERED EMBODYMENTS

Referring to Fig. 1, Fig. 2 and such, the preferred modes of the present invention are described. The present mode represents one example of the semiconductor device having an input/output protection circuit section that contains a CMOS. Fig. 1 is a plan view showing an input protection circuit section in accordance with the present invention, and Fig. 2, a cross-sectional view showing the portion A-A' of Fig. 2. As shown in Fig. 2, a CMOS of the present embodiment has a twin-well structure in which an N-type well 1b and a P-type well 2 are formed, adjoining each other on the surface of a P-type silicon substrate 20. The dopant concentration of the N-type well 1b and the P-type

well 2 are set, for example, to be 1.0×10^{17} to 1.0×10^{18} cm^{-3} or so. Further, while the present embodiment employs the twin-cell structure, the semiconductor device of the present invention is not limited to use such a structure and is able to utilize any of various well structures including a single-well and triple-well structures.

As shown in Fig. 2, an N-channel MOSFET is formed in the region where the P-type well 2 is formed. The N-channel MOSFET comprises a gate electrode 6, a source region 3c, a drain region 3b and an extension region 12. The extension region 12 as used herein indicates the region where the dopant concentration is lower than that of the source-drain regions. For instance, while the dopant concentrations of the source region 3c and the drain region 3b are 1.0×10^{20} cm^{-3} or so, the dopant concentration of the extension region is 1.0×10^{19} cm^{-3} or so. Further, between the gate electrode 6 and the substrate, there is set a gate insulating film. As the gate insulating film, in addition to a silicon oxide film, a silicon nitride film, a silicon oxynitride film or a film made of a high dielectric material such as tantalum oxide (Ta_2O_5) may be utilized.

In the periphery of the N-channel MOSFET formation area, a P-type dopant diffusion region 4a is set (Fig. 1), and thereby the electric potential of the P-type well 2 is defined. The P-type dopant diffusion region 4a and the source region 3c, set separated by an element isolation film

10, are both connected with a ground terminal 9 (GND). The drain region 3b is connected with an input terminal 7. Under the source region 3c and the element isolation film 10, an N-type well 1a is formed. The dopant concentration of the N-type well 1a is set to be lower than the dopant concentration of the overlying source region 3c. As the dopant concentration of the N-type well 1a, 1.0×10^{17} to 1.0×10^{18} cm^{-3} is appropriate.

Meanwhile, in the region where the N-type well 1b is formed, a P-channel MOSFET comprising a gate electrode 5, a source region 4c, a drain region 4b and an extension region 11 is formed. Regarding the dopant concentrations of respective regions, description of the gate insulating film and such, the same as the N-channel MOSFET can be employed to form the analogous structure. If the dopant concentration of the N-type well 1b and the N-type well 1a are set to be the same, these wells can be formed in one and the same step, which is advantageous to simplify the steps of a manufacturing method. In the periphery of the P-channel MOSFET formation area, an N-type dopant diffusion region 3a is set (Fig. 1), and thereby the electric potential of the N-type well 1b is defined. The N-type dopant diffusion region 3a and the source region 4c, set separated by an element isolation film 10, are both connected with a supply terminal 8 (V_{DD}). The drain region 4b is connected with an input terminal 7.

Further, for the purpose of lowering the parasitic resistance and such, silicide layers 13 are formed over the surfaces of the source-drain regions and such, in every transistor. The silicide layers 13 are made of a material such as titanium silicide, cobalt silicide and the like.

Next, operations that the N-channel MOSFET makes when an external surge is applied through the input terminal 7 to the protection circuit section with the above structure are described.

Firstly, when a negatively polarized surge with respect to the ground terminal 9 is applied to the input terminal 7, a forward voltage is applied to the PN-junction between the drain region 3b (N-type) and the P-type well 2 and the PN diode is turned on in the forward direction so that the negatively polarized surge flows down from the input terminal 7, through the drain region 3b and the P-type well 2, to the ground terminal 9. Next, when a positively polarized surge with respect to the ground terminal 9 is applied to the input terminal 7, a positive voltage with respect to the P-type well of the N-channel transistor is applied to the drain. When this voltage exceeds a certain value, an avalanche breakdown takes place in the vicinity of the drain region 3b. After the breakdown, a hole current flows from the drain region 3b to the P-type well 2 and this current leads the P-type well 2 to have a positive electric potential, which results in turning-on of an NPN parasitic

bipolar transistor in which the drain region 3b, the P-type well 2 and the source region 3c act as a collector, a base and an emitter, respectively. The surge, then, flows from the internal terminal 7, through the drain region 3b, the P-type well 2 and the source region 3c, and consequently to the ground terminal 9. Since the N-type well 1a is formed under the source region 3c in the present embodiment, the electric potential of the base region of the NPN parasitic bipolar transistor (the P-type well 2 under the gate electrode 6 in Fig. 2) becomes easily raised after the breakdown. This can be explained in the following way. Namely, because a hole current generated due to the breakdown starts flowing along the current path through the silicon substrate 20 of a high resistivity, as indicated by the arrow in Fig. 5, the electric potential of the base region of the parasitic bipolar transistor increases as much as the voltage drop brought about through the silicon substrate 20 of a high resistivity. As the potential of the base region of the parasitic bipolar transistor readily increases in this manner, the snap-back can be easily induced thereto.

The operations described above are further described with reference to Fig. 4. In Fig. 4, when the drain voltage reaches the breakdown voltage V_B, the breakdown takes place and, after that, the voltage rises up to the trigger voltage V_{t1}. The value of V_{t1} is smaller than that of the

conventional one, as described above. After the NPN parasitic bipolar transistor is turned on, the voltage drops to V_S. Thereafter the current and the voltage rise again and reach the transistor failure current I_{t2} and the transistor failure voltage V_{t2}, respectively. As V_{t1} is lowered, the condition $V_{t1} < V_{t2}$ holds. Under this condition, even if only some of the transistors are induced to make the snap-back operation first, the rest of the transistors can be also induced to make the snap-back operation in the similar fashion, as the drain voltage, after the snap-back, increases from V_S to V_{t2}. In this manner, in the protection circuit section of the present embodiment, a plurality of transistors composing the protection circuit section all function alike. Therefore, more than sufficient ESD-proof can be secured, without lowering protective capability thereof.

In the present embodiment, the ESD-proof is increased without setting a high resistance region so that high-speed operations become possible, and the response of the protection circuit become faster than obtained so far. In addition, the drain current of the transistor is not lowered, and a sufficient driving current can be readily secured even in the output circuit or the like. Further, since no additional resistance element is disposed between a gate and a contact in the drain region of the protection circuit section, the spacing between gates can be narrowed

and the element size of the input/output protection circuit section can be reduced, which is an advantage to make miniaturization of the LSI.

As described above, the present invention establishes the relationship

V_{t1} (trigger voltage) < V_{t2} (transistor failure voltage),

by setting an N-type well 1a, instead of employing the conventional method wherein a high-resistance region is set. In other words, in place of increasing V_{t2} by setting a high-resistance region, V_{t1} is decreased by setting an N-type well 1a and thereby the above condition is established. While the above relationship can be obtained solely by means of setting an N-type well 1a, it is preferable to make the difference between V_{t2} and V_{t1} as large as possible so as to enhance the reliability of the protection circuit section. Especially when the structure in which silicide layers are set on the surfaces of the source-drain regions and such of the transistor is employed, failures of the transistors become more liable to happen owing to the surge gathering, and, therefore, increasing the difference between V_{t2} and V_{t1} gains in importance further. In this respect, it is more effective if an additional arrangement described below is made. That is, (i) the gate length or the length of the gate electrode 6 as seen in Fig. 2 is set to be not greater than 0.2 μm, or alternatively, (ii) a first and second

diffusion layers (the source region 3c and the drain region 3b in the present embodiment) are each made to have an extension structure. Such an arrangement together with setting an N-type well 1a produces the multiplication effect, and the parasitic bipolar transistor composed of the source region 3c, the P-type well 2 under the gate electrode 6 and the drain region 3b becomes more easily turned on so that V_{t1} can be lowered with effect. The extension structure as used herein indicates a structure wherein dopant diffusion regions with a lower dopant concentration than the source-drain regions are set at end sections of the source-drain regions on the side of the channel layer, and this structure may be formed by oblique rotational ion implantation. As the dopant concentration of the extension region, 1.0×10^{19} cm^{-3} to 1.0×10^{20} cm^{-3} is appropriate.

Further, although the element isolation film 10 is set between the source region 3c and the P-type dopant diffusion region 4a in the present embodiment, the source region 3c and the P-type dopant diffusion region 4a can be placed next to each other without setting this element isolation film therebetween. Such an arrangement can further reduce the size of the protection circuit section. In the conventional techniques, the distance between the P-type dopant diffusion region 4a and the channel layer of the N-channel MOSFET is set considerably large, and besides, in order to increase the resistance therebetween, the element isolation film 10

described above is set therein. Without this arrangement, the electric potential of the base region (the P-type well 2 under the gate electrode 6) of the parasitic bipolar transistor cannot be raised sufficiently high and it is difficult to bring about the snap-back. In contrast with this, in the present invention, with the N-type well 1a being set, the snap-back operation of the parasitic bipolar transistor can be readily induced, even if the distance between the P-type dopant diffusion region 4a and the N-channel MOSFET is short. Accordingly, in the case that the structure of the present invention is employed, it is possible to dispose the source region 3c and the P-type dopant diffusion region 4a next to each other, without setting the element isolation film 10 at all.

While an example in which the N-type well is formed in the N-channel MOSFET is shown in the present embodiment, a P-type well can be set under the source region 4c of the P-channel MOSFET. In this instance, however, it is preferable that either the P-type well is formed not so deep as the N-type well 1b or an N-type substrate is employed therefor.

Further, in the present embodiment, there is shown an example with the protection circuit section that contains a CMOS structure section, but a protection circuit section composed of solely a plurality of MOSFETs can be employed. Further, although the present embodiment is described, taking an input circuit protection section as an example, it

is to be understood that the present invention may be also applied to output circuit protection section.

Examples

Example 1

Referring to the drawings, the present example is described. Fig. 1 is a plan view showing an input protection circuit section of the present example and Fig. 2, a cross-sectional view showing the portion A-A' of Fig. 1. As shown in Fig. 2, on the surface of a P-type silicon substrate 20, an N-type well 1b (with a phosphorus concentration of $10^{17}/cm^3$ or so) and a P-type well 2 (with a boron concentration of $10^{17}/cm^3$ or so) is formed. In the region where the P-type well 2 is formed, an N-channel MOSFET comprising a gate electrode 6, a source region 3c, a drain region 3b and an extension region 11 is formed. In the periphery of the N-channel MOSFET formation area, a P-type dopant diffusion region 4a is set (Fig. 1), and thereby the electric potential of the P-type well 2 is defined. The P-type dopant diffusion region 4a and the source region 3c, set separated by an element isolation film 10, are both connected with a ground terminal 9 (GND). The drain region 3b is connected with an input terminal 7. Under the source region 3c and the element isolation film 10, an N-type well 1a (with a phosphorus concentration of $10^{17}/cm^3$ or so) is formed. In the present example, the N-type well 1a, the N-type well 1b and the P-type well 2 all have a depth of 1 μm

or so.

Further, the extension region of the N-channel MOSFET is formed to have an arsenic concentration of 1×10^{19} cm^{-3}.

Meanwhile, in the region where the N-type well 1b is formed, a P-channel MOSFET comprising a gate electrode 5, a source region 4c, a drain region 4b and an extension region 11 is formed. The N-type well 1b has a phosphorus concentration of $1\times10^{17}/cm^3$ or so, as the N-type well 1a. In the periphery of the P-channel MOSFET formation area, an N-type dopant diffusion region 3a is set (Fig. 1), and thereby the electric potential of the N-type well 1b is defined. The N-type dopant diffusion region 3a and the source region 4c, set separated by an element isolation film 10, are both connected with a supply terminal 8 (V_{DD}). The drain region 4b is connected with an input terminal 7.

The gate electrodes 5 and 6 are formed over a silicon oxide film on the substrate. The width of each gate electrode (gate length) is set to be 0.2 μm.

Further, for the purpose of lowering the parasitic resistance and the like, silicide layers 13 made of cobalt silicide are formed over the surfaces of the source-drain regions and such, in every transistor. Formation of these silicide layers 13 is carried out by forming, first, a cobalt film using the sputtering method and then applying a heat treatment thereto.

Next, operations of the protection circuit section

with the above structure are described. When an external surge is applied to the input terminal 7, the surge flows down along either a path through the N-channel MOSFET and the ground terminal 9 or a path through the P-channel MOSFET and the supply terminal 8 so that the internal circuit may be protected. Since the N-type well 1a is formed under the source region 3c in the present example, the electric potential of the base region of the NPN parasitic bipolar transistor (the P-type well 2 under the gate electrode 6) becomes easily raised after the breakdown. Consequently, with the trigger voltage of Fig. 4 being lowered, the relationship $V_{t1} < V_{t2}$ is established. Under this condition, even if only some of the transistors are induced to make the snap-back operation first, the rest of the transistors are also induced to make the snap-back operation in the similar fashion, as the drain voltage, after the snap-back, increases from V_S to V_{t2}, and, thus, a plurality of transistors all function alike, and, as a result, the ESD-proof is improved. In a semiconductor device of the present example, the trigger voltage V_{t1} and the transistor failure voltage V_{t2} are approximately 6V and 9V, respectively.

In the present example, as a high-resistance region of the drain section is not set, the response of the protection circuit is made faster and high-speed operations can be realized. In addition, the drain current of the transistor

is not lowered, and a sufficient driving current can be readily secured even in the output circuit. Further, since no additional resistance element is disposed between a gate and a contact, the spacing between gates can be narrowed and the width of the input/output protection circuit section or the distance between B-B′ of Fig. 1 can be reduced a great deal. With the conventional technique shown in Fig. 11, if 8 lines of the gates are provided, the required width of the input/output protection circuit section is approximately 50 μm. As against this, in the present example, for the same number of gates, the width can be reduced down to approximately 25 μm.

Comparative Example 1

Fig. 8 shows a cross-sectional structure of a semiconductor device of the present Comparative Example. In this semiconductor device, under a control gate, an N-type well 1c is set and an internal terminal 7 is connected with an N-type diffusion region 3d. In this point, the present Comparative Example differs from the semiconductor device of Example 1, in which the input terminal 7 is connected with the drain region 3b and the input terminal 7 and the NMOSFET therein makes direct connection and not through a high-resistance region. Further, in this semiconductor device, no extension regions are provided to the source-drain regions, which is another point differing from Example 1. Except these differences, a semiconductor device was made in

the same way as Example 1.

For the semiconductor device of the present Comparative Example, V_{t1} and V_{t2} are approximately 8V and 12V, respectively, and this value of $V_{t1}$is higher than that of Example 1. It is considered that the inducing effect that N-type well 1a has on the operations of the parasitic bipolar transistor is weakened by the resistance component of the N-type well 1c. Further, the width of the input/output protection circuit section remains approximately 50 μm for 8 lines of the gates and a reduction of the size of the protection circuit was by no means accomplished.

Example 2

Fig. 3 shows a cross-sectional structure of an input protection circuit section of the present example. This input protection circuit section is an example in which dopant high-concentration regions or so-called retrograde wells 15 and 16 are formed, at bottom sections of the N-type well 1b and the P-type well 2 in the CMOS of Fig. 2, respectively. The formation of the retrograde wells is performed by conducting ion implantation a plurality of times under different conditions of an injection energy and a dose but using the same mask. In the present example, a phosphorus concentration of 1×10^{17} cm^{-3} or so is employed for the N-type wells 1b and 1a, and a boron concentration of 1×10^{17} cm^{-3} or so, for the P-type well 2. Further, a

phosphorus concentration for the dopant high-concentration region 15 is set to be 2×10^{17} cm^{-3} or so and a boron concentration for the dopant high-concentration region 16, 2×10^{17} cm^{-3} or so.

It is well known that setting a dopant high-concentration region can reduce the shunt resistance and improve the latch-up-proof but, in the conventional techniques, this also brings about a problem of lowering the ESD-proof. In contrast with this, because the N-type well 1a is set under the source region 3c in the present example, after the breakdown of the drain region 3b occurs in the N-channel MOSFET, a hole current starts flowing down along a current path through the silicon substrate 20 that has a high electric resistance. This facilitates the electric potential of the base region of the lateral parasitic bipolar transistor to increase and, at the same time, can reduce the trigger voltage V_{t1} so that the ESD-proof is improved. Meanwhile, in the internal circuit region (not shown in the drawing), because the shunt resistance is made smaller by the dopant high-concentration regions 15 and 16, the proof is a good deal improved against latch-up that may occur between the input/output protection circuit section and the internal circuit region. In the semiconductor device of the present example, even an injection of a current of 500 mA or more into the input/output terminal did not bring about latch-up.

As described above, the semiconductor device of the present invention has, under a first diffusion layer that constitutes a transistor of a protection circuit section, a first conductive type well with a dopant concentration lower than that of the first diffusion layer so that it becomes easier to induce operations of a lateral parasitic bipolar transistor composed of source-drain regions and a channel layer of the afore-mentioned transistor. Consequently, a protection circuit having a high response speed and an excellent ESD-proof can be obtained. In addition, the semiconductor device of the present invention has a structure in which a second diffusion layer of the afore-mentioned transistor is connected with an input/output terminal section and, unlike the prior art, a high-resistance region is not set, the drain current of the transistor is not lowered, and a sufficient driving current can be readily secured even in the output circuit or the like. Further, the spacing of the gates in the protection circuit section can be narrowed and, thus, further miniaturization of the input/output protection circuit section can be made.

Further, in case that the input/output protection circuit section comprises a complementary field effect transistor, a surge can flow down through a plurality of lines efficiently, which provides another advantage of

attaining further improvement of the ESD-proof. In this instance, by employing a structure in which a dopant high-concentration region is set beneath wells that constitutes the transistor, and the depth of the afore-mentioned first conductive type well is set deeper than the level at which the dopant high-concentration region is formed, a protection circuit section having a good ESD-proof, together with a good latch-up-proof, can be obtained.

This application is based on Japanese patent application NO.HEI11-209407, the content of which is incorporated hereinto by reference.

what is claimed is :

1. A semiconductor device having an input/output protection circuit section on a semiconductor substrate; wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type and a gate electrode that is set in the region sandwiched between these layers; and

a dopant diffusion region of second conductive type is set at a distance from the region where said plurality of field effect transistors are formed; and

while said dopant diffusion region is connected with a reference potential, the second diffusion layer is connected with an input/output terminal section; and

under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

2. The semiconductor device according to Claim 1, wherein said gate electrode and said dopant diffusion region of second conductive type are placed over the second conductive type well that is formed on the surface of the semiconductor substrate; and the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level

deeper than the bottom of the second conductive type well.

3. The semiconductor device according to Claim 1, wherein said field transistors are N-channel type field effect transistors.

4. A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section that contains a complementary field effect transistor; wherein:

said complementary field effect transistor is composed of a first field effect transistor having a first and second diffusion layers of first conductive type and a gate electrode that is set in the region sandwiched between these layers and a second field effect transistor having a third and fourth diffusion layers of second conductive type and a gate electrode that is set in the region sandwiched between these layers; and

a first dopant diffusion region of second conductive type is set at a distance from the region where said first field effect transistor is formed, and a second dopant diffusion region of first conductive type is set at a distance from the region where said second field effect transistor is formed; and

the first dopant diffusion region is connected with a first reference potential; the second dopant diffusion region, with a second reference potential; and the second

diffusion layer and the fourth diffusion layer are each connected with an input/output terminal section; and

under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

5. The semiconductor device according to Claim 4, wherein the gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate; and the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

6. The semiconductor device according to Claim 5, wherein, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well; and the bottom of said first conductive type well is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. The semiconductor device according to Claim 4, wherein the first field transistor is an N-channel type field effect transistor.

ABSTRACT

In an N-channel type field effect transistor constituting an input/output protection circuit, an N-type well 1a with a lower dopant concentration than the source region 3c is formed under the source region 3c.

Fig. 1

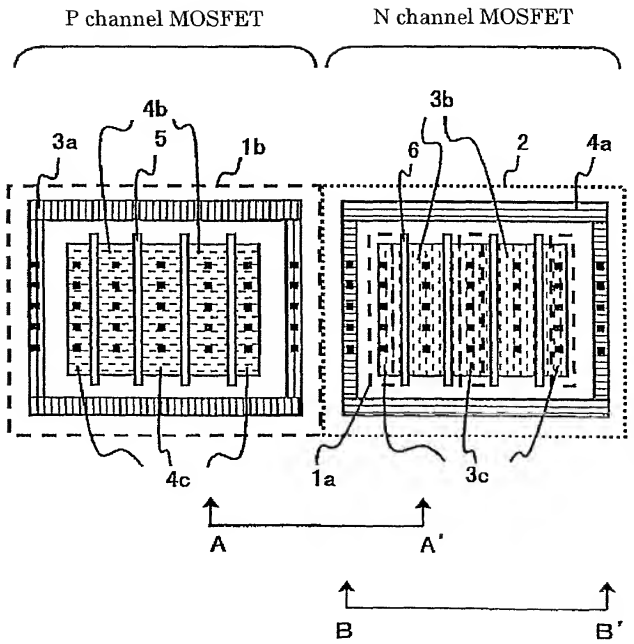
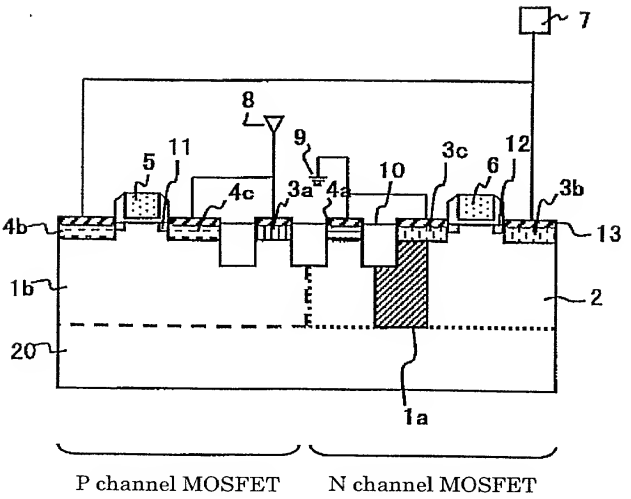

P channel MOSFET
N channel MOSFET
3a
4b
5
1b
3b
6
2
4a
4c
1a
3c
A
A'
B
B'

Fig. 2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8
9
5
11
4c
3a
4a
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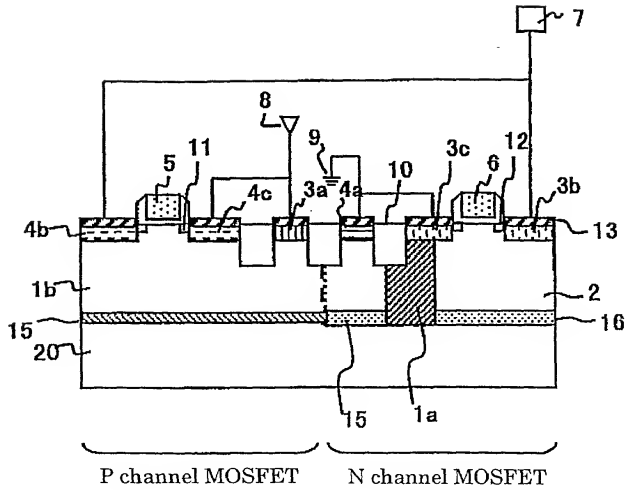
3c
6
12
3b
4b
13
1b
2
20
1a
P channel MOSFET
N channel MOSFET

Fig. 3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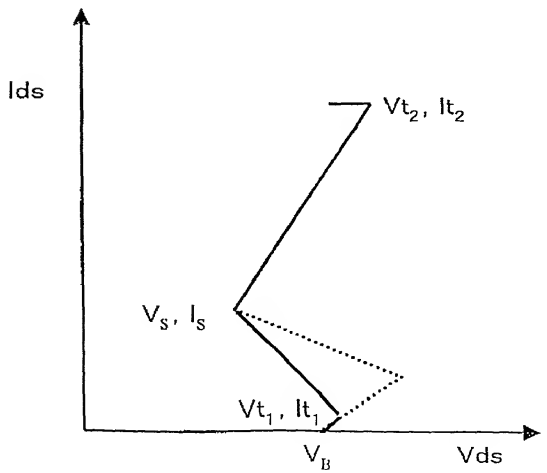
9
11
5
4c
3a
4a
10
3c
6
12
3b
4b
13
1b
2
15
16
20
15
1a
P channel MOSFET
N channel MOSFET

Fig. 4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V_S, I_S
Vt_1, It_1
V_B
Vds

Fig. 5

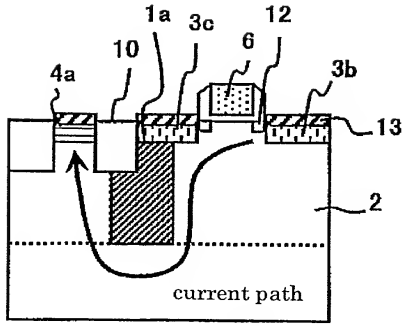

1a
3c
12
10
6
4a
3b
13
2
current path

Fig. 6

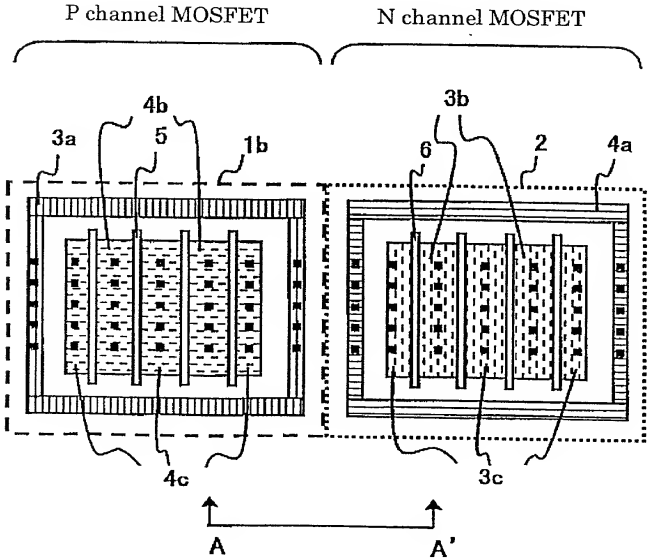
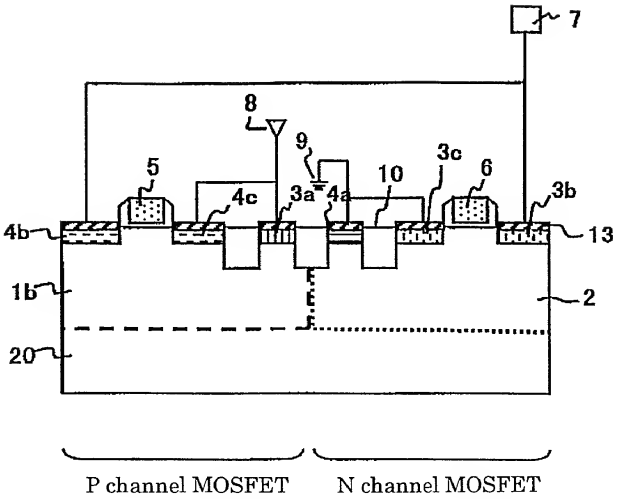

P channel MOSFET
N channel MOSFET
4b
3a
5
1b
3b
6
2
4a
4c
3c
A
A'

Fig. 7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8
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5
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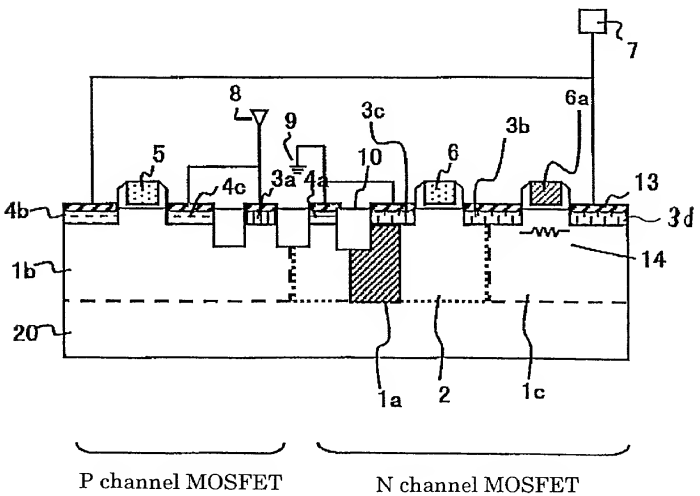
20
P channel MOSFET
N channel MOSFET

Fig. 8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4b
3d
14
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1a
2
1c
P channel MOSFET
N channel MOSFET

Fig. 9

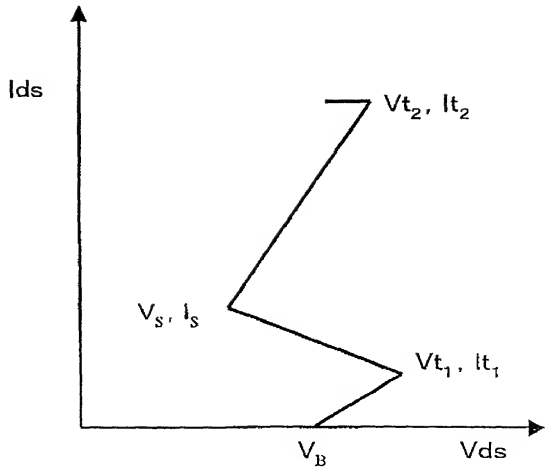

Ids
Vt2, It2
VS, IS
Vt1, It1
VB
Vds

Fig. 10

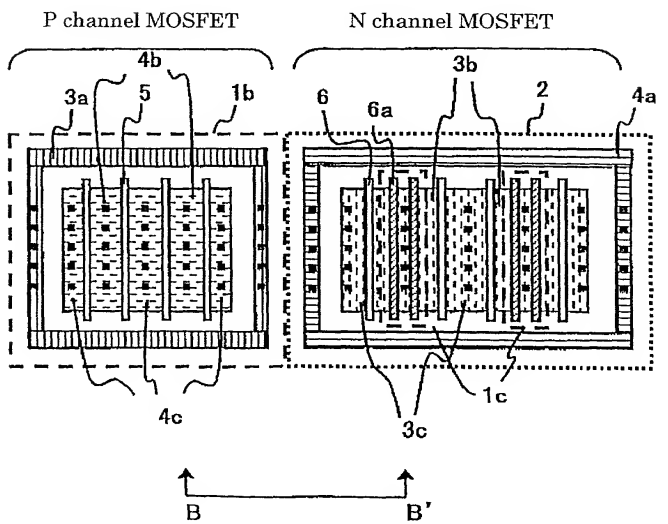
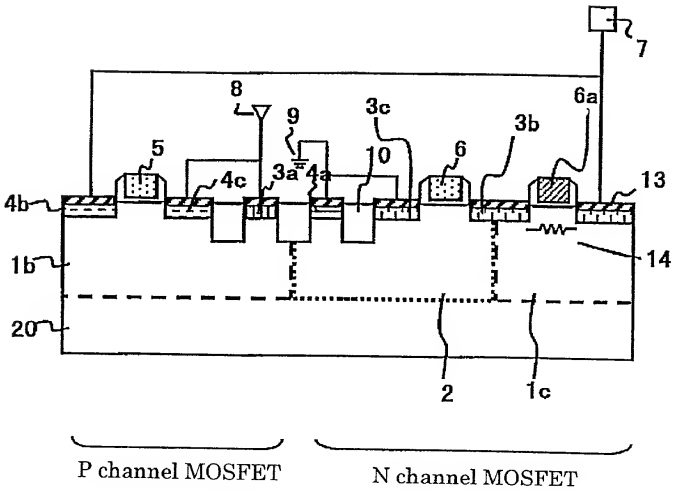

P channel MOSFET
N channel MOSFET
4b
3a
5
1b
6
6a
3b
2
4a
4c
3c
1c
B
B'

Fig. 11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3b
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3a
4a
13
4b
14
1b
20
2
1c
P channel MOSFET
N channel MOSFET

Fig. 12

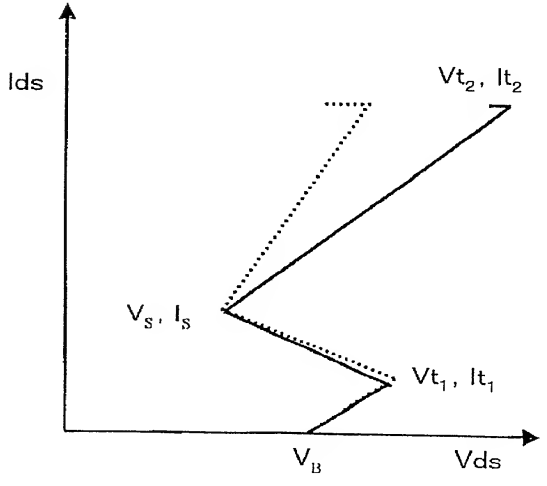
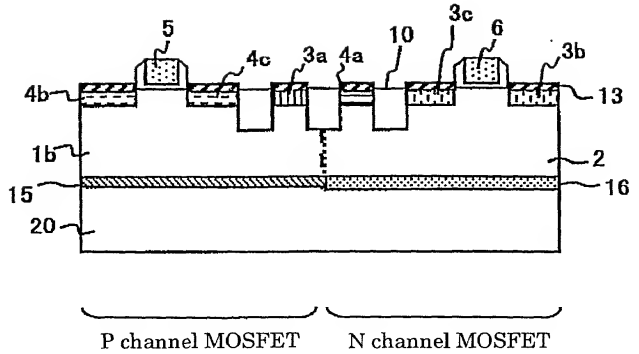

Ids
Vt2, It2
VS, IS
Vt1, It1
VB
Vds

Fig. 13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4c
3a
4a
10
3c
6
3b
4b
13
1b
2
15
16
20
P channel MOSFET
N channel MOSFET

Fig. 14

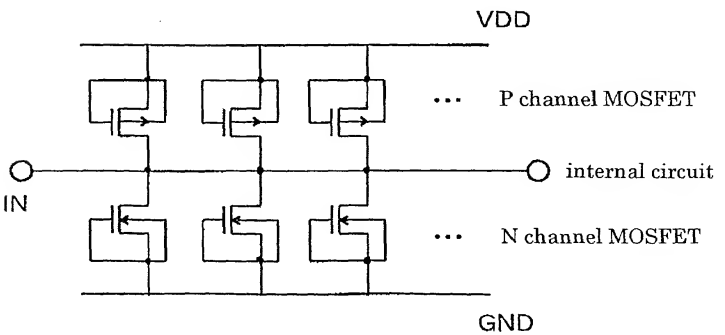
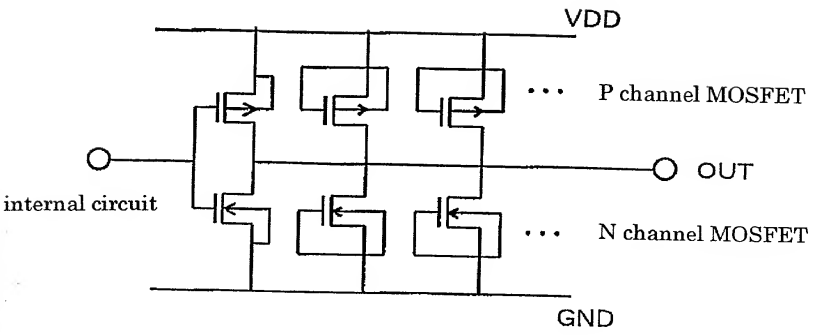

VDD
P channel MOSFET
internal circuit
IN
N channel MOSFET
GND

Fig. 15


VDD
P channel MOSFET
OUT
internal circuit
N channel MOSFET
GND

Docket No. _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE

the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

NUMBER	COUNTRY	DAY/MONTH/YEAR FILED	PRIORITY CLAIMED
11-209407	Japan	23/07/1999	yes

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

APPLICATION NO.	FILING DATE

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112. I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

I hereby appoint as my attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Stephen A. Bent, Reg. No. 29,768; David A. Blumenthal, Reg. No. 26,257; John J Feldhaus, Reg. No. 28,822; Donald D. Jeffery, Reg. No. 19,980; Eugene M. Lee, Reg. No. 32,039; Peter G. Mack, Reg. No. 26,001. Brian J. McNamara, Reg. No. 32,789; Sybil Meloy, Reg. No. 22,749; George E. Quillin, Reg. No. 32,792; Colin G. Sandercock, Reg. No 31.298; Bernhard D. Saxe, Reg. No. 28,665; Charles F. Schill, Reg. No. 27,590; Richard L. Schwaab, Reg. No. 25,479; Arthur Schwartz. Reg. No. 22,115; Harold C. Wegner, Reg. No. 25,258.

Docket No._____

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor	Signature of First or Sole Inventor	Date
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